CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

IN THE CLAIMS

1. (currently amended) An integrated circuit comprising:

a configurable function unit including a configurable function unit component; and

at least one configurable decoder having decoder configuration data and a decoder output, the configurable decoder being operable to decode a value in data presented by the configurable function unit component;

wherein the configurable decoder is optimized to assert the decoder output based on a comparison of the decoder configuration data with the value presented by the configurable function unit component;

wherein the decoder configuration data is specified by configuring decoder cells having cell values of binary logic one, and binary logic zero;

wherein the decoder output is asserted when the value presented by the configurable function unit component are consistent with the cell values; and

wherein the decoder cells can further have cell values of "don't care".

2-3. (canceled)

4. (original) The integrated circuit of claim 1, wherein the configurable function unit is a first configurable function unit, further comprising a second configurable function unit, wherein a cascade output of the configurable decoder is provided to the second configurable function unit to facilitate combining the first configurable function unit with the second configurable function unit.

5. (original) The integrated circuit of claim 4, wherein the cascade output is the decoder output.

6. (original) The integrated circuit of claim 1, wherein the integrated circuit is a field programmable gate array (FPGA) including at least one look-up table.

7. (original) The integrated circuit of claim 1, wherein the integrated circuit is a complex programmable logic device (CPLD) having a plurality of function blocks, the function blocks including a plurality of macrocells.

8. (original) The integrated circuit of claim 7, wherein the configurable function unit is associated with a predetermined function block of the function blocks of the CPLD.

9. (original) The integrated circuit of claim 8, wherein the configurable function unit is logically contained within a predetermined macrocell in the macrocells.

10. (original) The integrated circuit of claim 9, wherein the decoder output is synchronized with the CPLD by way of a macrocell register associated with the predetermined macrocell.

11. (original) The integrated circuit of claim 9, wherein the predetermined macrocell of the macrocells has a set of control inputs that are substantially congruent with the control inputs of the remainder of the macrocells in the predetermined function block.

12. (original) The integrated circuit of claim 9, wherein when it operates as a specialized macrocell, the predetermined macrocell of the macrocells utilizes control inputs that are substantially the same as the control inputs it utilizes when operating as a standard macrocell.

13. (original) The integrated circuit of claim 9, wherein the predetermined macrocell in the macrocells is a buried macrocell.

14. (original) The integrated circuit of claim 7, wherein an input of the configurable function unit comprises a configurable product term.

15. (original) The integrated circuit of claim 1, wherein the configurable function unit component is a counter.

16. (original) The integrated circuit of claim 15, wherein the configurable decoder is operable to match a predetermined value one clock cycle before the configurable function unit component reaches the predetermined value.

17. (original) The integrated circuit of claim 15, wherein the configurable decoder is operable to match a specified terminal value and, based on reaching the specified terminal value, to cause a reset of the configurable function unit component.

18. (original) The integrated circuit of claim 17, wherein the reset is an asynchronous reset.

19. (original) The integrated circuit of claim 15, wherein the decoder output is synchronized and provided to the logical interconnection network.

20. (original) The integrated circuit of claim 1, wherein the configurable function unit component is a shift register.

21. (original) The integrated circuit of claim 20, wherein the configurable decoder is operable to match a predetermined value within the shift register one clock cycle before the shift register contains a particular shift register value by decoding all bits in the shift register excluding the most significant bit and concatenated with the bit value of a shift-in input to the shift register.

22. (original) The integrated circuit of claim 1, wherein the configurable function unit component is a cyclic redundancy check generator (CRC generator).

23. (original) The integrated circuit of claim 1, wherein the configurable function unit component is a serial encrypter.

24. (original) The integrated circuit of claim 1, wherein the configurable function unit component is a feedback shift register.

25. (original) The integrated circuit of claim 1, wherein the configurable function unit component is an accumulator.

26. (previously presented) A programmable logic device comprising:

programmable logic;

a counter providing a counter value;

a decoder configurable to provide an output signal in response to a selected counter value; and

an interconnect matrix for interconnecting the programmable logic, and receiving the output signal;

wherein the decoder comprises decoder cells capable of having decoder cell values of one, zero, and "don't care".

27. (canceled)

28. (original) The programmable logic device of claim 26, wherein a cascade output of the decoder is provided to the programmable logic device to facilitate combining the counter with at least one other counter in the programmable logic device.

29. (original) The programmable logic device of claim 28, wherein the cascade output is the output signal, and the decoder is configured to provide the cascade output when the counter value is all logical ones.

30. (original) The programmable logic device of claim 29, wherein the cascade output is asserted one clock cycle before the counter value is all logical ones.

31. (original) The programmable logic device of claim 26, wherein the decoder is configured with a terminal count whereby the counter is reset when the counter value matches the terminal count.

32. (original) The programmable logic device of claim 31, wherein the terminal count is decoded one clock cycle before the terminal count is reached.

33. (original) The programmable logic device of claim 31, wherein the counter is reset synchronously.

34. (original) The programmable logic device of claim 31, wherein the counter is reset asynchronously.

35. (original) The programmable logic device of claim 31, wherein the counter is controlled by a clock enable.

36. (original) The programmable logic device of claim 26, wherein the programmable logic device is a field programmable gate array (FPGA) including at least one look-up table.

37. (original) The programmable logic device of claim 26, wherein the programmable logic device is a complex programmable logic device (CPLD) having a plurality of function blocks, the function blocks including a plurality of macrocells.

38. (previously presented) A programmable logic device comprising:

programmable logic;

a shift register providing a shift register value;

a decoder configurable to provide an output signal in response to a selected shift register value; and

an interconnect matrix for interconnecting the programmable logic, and receiving the output signal;

wherein the decoder comprises decoder cells capable of having decoder cell values of one, zero, and "don't care".

39. (canceled)

40. (original) The programmable logic device of claim 39, wherein a shift cascade output of the decoder is provided to the programmable logic device to facilitate combining the shift register unit with at least one other shift register in the programmable logic device.

41. (original) The programmable logic device of claim 40, wherein the shift cascade output is the output signal and the decoder is configured with "don't care" cells in all but a most significant bit of the decoder cell values, and with a one in the most significant bit of the decoder cell values, whereby the decode result represents the most significant bit in the shift register unit as the most significant bit in the shift register unit is shifted out of the shift register unit.

42. (original) The programmable logic device of claim 41, wherein the shift cascade output corresponds to the next-to-most-significant bit in the shift register.

43. (original) The programmable logic device of claim 38, wherein the programmable logic device is a field programmable gate array (FPGA) including at least one look-up table.

44. (original) The programmable logic device of claim 38, wherein the programmable logic device is a complex programmable logic device (CPLD) having a plurality of function blocks, the function blocks including a plurality of macrocells.

45. (currently amended) A CPLD having interconnectable programmable logic, configuration memory, and external inputs and outputs, the interconnectable programmable logic being connected by a logical interconnection matrix and the CPLD comprising:

a configurable function unit including a configurable function unit component; and

a configurable decoder operable to assert a decoder output upon detecting a decode value in data presented by the configurable function unit component;

wherein the configurable function unit is logically internal to a predetermined specialized macrocell logically within the predetermined function block; and

wherein the decoder output is synchronized by and provided to the rest of the CPLD through a macrocell register associated with the predetermined specialized macrocell.

46. (original) The CPLD of claim 45, wherein a decoder configuration associated with the configurable decoder comprises decoder cells, which are configured to match output bits of the configurable function unit component corresponding to binary logic one, binary logic zero, and corresponding to a value that matches either binary logic one, binary logic zero, or that matches both binary logic one and binary logic zero.

47. (original) The CPLD of claim 45, wherein the configurable function unit is logically internal to a predetermined function block of the CPLD.

48-49. (canceled)

50. (currently amended) The CPLD of claim 45 ~~48~~, wherein the decoder output is provided via a value rail to at least one macrocell in the predetermined function block other than the predetermined specialized macrocell.

51. (currently amended) The CPLD of claim 45 ~~48~~, wherein the decoder output is synchronized by and provided to the rest of the CPLD through a macrocell register in a macrocell other than the predetermined specialized macrocell.

52. (original) A programmable logic device having configuration memory and interconnectable programmable logic connected by a logical interconnection network, wherein at least a portion of the interconnectable programmable logic comprises macrocells, the programmable logic device comprising:

a configurable function unit including a function unit component and at least one configurable decoder programmable to decode a particular value as stored in the configuration memory when the particular value is presented by the function unit component, wherein the configurable function unit is located in a predetermined specialized macrocell of the programmable logic device; and

a plurality of logical function unit inputs associated with the predetermined specialized macrocell, the logical function unit inputs performing substantially the same functions as macrocell control inputs associated with the conventional macrocells.